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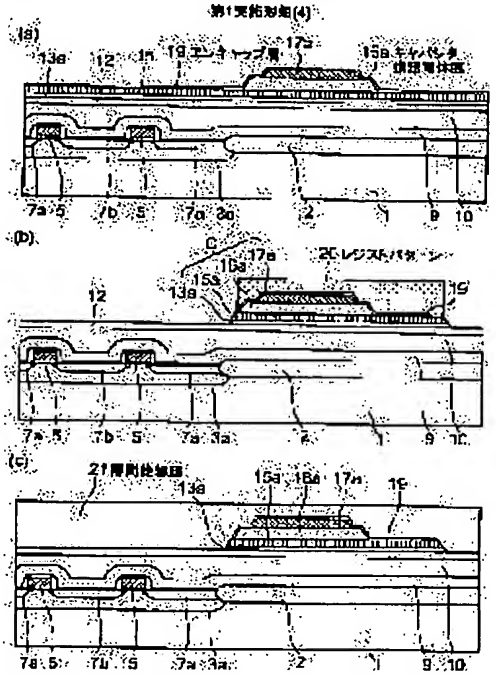
(54) SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To form a ferroelectric capacitor having a superior characteristic by a method for manufacturing a semiconductor device with a capacitor.
SOLUTION: The method includes the steps of forming a first insulation film 10 on a semiconductor substrate 1, planarizing an upper plane of the first insulation film 10, heating the first insulation film 10, forming a second insulation film 12 consisting of a silicon oxide film or a aluminum oxide film on the first insulation film 10, forming a titanium oxide film 13a on the second insulation film 12, forming a capacitor lower portion electrode 15a consisting of a platinum on the titanium oxide film 13, forming a capacitor ferroelectric film 16a on the capacitor lower electrode 15a, and forming an upper electrode 17a on the capacitor ferroelectric film 16a.



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[0001]
[Field of the Invention] This invention relates to the semiconductor device which has a capacitor, and its manufacture approach in more detail about a semiconductor device and its manufacture approach.

[0025] Next, drawing 3 (a) The SiO2 cap layer 12 for the purpose of [of a ferroelectric capacitor] a crystalline improvement is formed on the 1st interlayer insulation film 11 with a CVD method at the thickness of 130nm using TEOS so that it may be shown. Next, in order to form Pt/TiO2 laminating used as the lower electrode layer of a ferroelectric capacitor, the Ti film 13 with a thickness of 20nm is first formed on the SiO2 cap layer 12 by the spatter on the conditions shown in Table 1.

[0026]

[Table 1] gas pressure / power / time / temperature

	Arガス圧	DCパワー	時間	温度
Ti	0.15Pa	2.6kW	13秒	150℃

[0027] Then, drawing 3 (b) The Ti film 13 is oxidized thermally in O2 ambient atmosphere for 700 degrees C and 60 seconds using RTA (rapid thermal annealing) equipment, and the Ti film 13 is set to TiO2 film 13a of the rutile mold crystal structure so that it may be shown. The thickness of TiO2 film 13a formed of RTA processing of such conditions is set to 50nm. For creating TiO2 film 13a of this rutile mold crystal structure, although a reactant spatter is sufficient, the oxidizing [thermally] method by the elevated temperature of Ti film is desirable. In creation by the reactant spatter, since it is necessary to heat a silicon substrate 1 at an elevated temperature, a special spatter chamber configuration is needed. Furthermore, in the oxidation by RTA equipment, the crystallinity of TiO2 film becomes good rather than the oxidation at a general furnace. Because, according to oxidization by the usual heating furnace, Ti film which is easy to oxidize is once because it will be necessary to break it, in order to make the crystal structures other than [a lot of] the rutile mold crystal structure in low temperature. Therefore, it becomes advantageous in order that the direction of oxidation by RTA with a quick programming rate may form a good crystal.

[0028] In addition, when a nitride is used as a cap layer 12, it is in the inclination for the membraneous quality of the Ti film 13 on it not to be improved. Next, drawing 3 (c) Pt film with a thickness of 150nm which is the lower electrode 15 of a capacitor is formed by the spatter on TiO2 film 13a so that it may be shown. An example of the formation conditions of the lower electrode 15 is shown in Table 2.

[0029]

[Table 2]

	Arガス圧	DCパワー	時間	温度
Pt	0.6Pa	0.5kW	182秒	550℃

[0030] Next, drawing 4 (a) The PLZT (ferroelectric) film 16 with a thickness of 180nm is formed on the lower electrode layer 14 by the spatter on the conditions shown in Table 3 so that it may be shown.

[0031]

[Table 3]

	Arガス圧	RFパワー	時間
PLZT	0.7Pa	1.0kW	323秒

[0032] Furthermore, a silicon substrate 1 is put in into the mixed ambient atmosphere of Ar and O2 which is 2.5% of O2 concentration, and rapid heat treatment is performed for the PLZT film 16 which is ferroelectric film on condition that the programming rate of 125 degrees C from ordinary temperature / sec for 585 degrees C and 90 seconds. Thus, priority orientation of the crystal of the PLZT film 16 is carried out in the desirable <111> directions by placing the PLZT film 16 into an inert atmosphere, and crystallizing at low temperature.

[0033] Next, drawing 4 (b) The thickness it is thin in the up electrode layer 17 forms on the PLZT film 16 by the spatter on the conditions which show the oxidization iridium (IrO2) film which is 150nm in Table 4 so that it may be shown.

[0034]
[Table 4]

	ガス圧	Arガス流量	O2ガス流量	DCパワー	時間
IrO2	0.8Pa	100sccm	63sccm	2.0kW	26秒

[0035] Here, although it is for raising the hydrogen degradation resistance of the PLZT film 16, Pt film and SrRuO3 (SRO) may be used for having used IrO2 which is a conductive oxide as an up electrode layer 17. However, since a catalysis occurs to a hydrogen content child and it is [Pt is easy to generate a hydrogen radical, and returns the PLZT film 16 by this and] easy to degrade it, it is not so desirable. on the other hand, since IrO2 and SRO do not have a catalysis, they are hard to generate a hydrogen radical, and the hydrogen degradation resistance of the PLZT film 16 boils them markedly, and improves.
[0036] Subsequently, a silicon substrate 1 is set in the mixed ambient atmosphere of Ar and O2 of 1% of O2 concentration, and rapid heat treatment of the PLZT film 16 is performed on condition that 725-degree-C 20 seconds and the programming rate of 125 degrees C / sec. If the beginning is made to crystallize the PLZT film 16 in the low temperature of 585 degrees C as described above, orientation of the crystal of the PLZT film 16 will be carried out in the <111> directions. Furthermore, the oxygen defect in the crystal lattice of the PLZT film 16 is not only filled up, but eburnation happens to the PLZT film 16 by placing the PLZT film 16 into the oxygen ambient atmosphere of a minute amount, and heat-treating at hotter 725 degrees C.
[0037] By the way, if eburnation of the PLZT film 16 is performed before forming the up electrode layer 17 of IrO2, many air bubbles in the PLZT film 16 gather for one place and this is seen from a front face, it will be opened by the pinhole in the grain boundary section of the PLZT film 16, and is not desirable at that striped. On the other hand, if eburnation of the PLZT film 16 is heat-treated after depositing the up electrode layer 17 of IrO2, the surface dry area of the PLZT film 16 will be prevented, and a very flat IrO2/PLZT interface will be acquired. It is also guessed easily that the defect of the interface is decreasing. And Pb and PbO out of the PLZT film 16 by vapor pressure being high It can protect, when IrO2 blocks also to desorption.
[0038] After carrying out eburnation of the PLZT film 16 which is ferroelectric film as mentioned above, as shown in drawing 4 (c), the resist pattern 18 which has the pattern configuration of a capacitor up electrode is formed on the up electrode layer 17 which consists of IrO2, the resist pattern 18 is used as a mask, patterning of the up electrode layer 17 is carried out, and this is set to up electrode 17a of a capacitor. Then, a resist pattern 18 is removed.
[0039] Next, drawing 5 (a) A process until it forms the shown structure is explained. First, into O2 ambient atmosphere, a silicon substrate 1 is set and 650 degrees C and annealing for 60 minutes are performed. This annealing is for recovering the damage which went into the PLZT film 16 by the spatter and etching. Then, the resist pattern (un-illustrating) which has the pattern configuration of a capacitor ferroelectric is formed, this resist pattern is used as a mask, the PLZT film 16 is etched, and ferroelectric film 16a of a capacitor is formed for this.
[0040] After removing a resist pattern, in order to protect ferroelectric film 16a which tends to be returned by hydrogen, it forms in the thickness of 20nm by the spatter by using as the en cap layer 19 the PLZT film which is easy to carry out the trap of the hydrogen. Furthermore, rapid heat treatment of the programming rate of 125 degrees C / sec is carried out for the en cap layer 19 on 700-degree-C conditions for 60 seconds among O2 ambient atmosphere.
[0041] After that, it is drawing 5 (b). The resist pattern 20 which has the pattern configuration of a capacitor lower electrode is formed on the en cap layer 19, a resist pattern 20 is used as a mask, the en cap layer 19, the lower electrode layer 15, and TiO2 film 13a are etched, and the pattern of the lower electrode layer 15 obtained by this is set to lower electrode 15a of a capacitor so that it may be shown.
[0042] After removing a resist pattern 20, a silicon substrate 1 is placed into O2 ambient atmosphere, and recovery annealing of 650 degrees C and ferroelectric film 16a which consists of PLZT the condition for 60 minutes is performed. The capacitor C of a memory cell field is formed of lower electrode 15a in which patterning was carried out by the above process,

ferroelectric film 16a, and up electrode 17a.

0063] As mentioned above, although the case where could apply this invention also when a Pt/Ti laminated structure is used as for example, a lower electrode which is not what is restricted to the above-mentioned operation gestalt, and PZT and PLZT were used as a ferroelectric ingredient although explained in accordance with the operation gestalt was mainly explained, other ferroelectric ingredients can also be used. For example, SBT, SBTN, etc. may be used. moreover -- although the above-mentioned operation gestalt mainly explained the case where the ferroelectric film was formed by the spatter -- other membrane formation approaches, for example, a sol gel process, and MOCVD -- law etc. can be used. In addition, probably, it will be obvious to this contractor for various modification, amelioration, and combination to be possible.

[0075] in addition -- although PLZT was used as ferroelectric film -- other PZT(s) or PZT system ingredients, and SrBi2Ta 2O9 and SrBi2(Ta, Nb)2O9 etc. -- Bi layer structure compound etc. may be used. Moreover, formation of the above-mentioned lower electrode may be adopted also in the capacitor using the high dielectric materials of an oxide.
[0076]
[Effect of the Invention] Since it was made to add on the insulator layer which gave CMP and performed degasifying processing further according to this invention as stated above before forming the lower electrode layer for capacitors for the process which forms an insulator layer once again The peak (002) of Ti film formed on the insulator layer can be strengthened, a possibility that **** of Pt which is moreover a lower electrode layer may arise disappears, and the particle size of Pt film can make the crystallinity of Pt good in 100-150nm and the large condition. Moreover, by the ferroelectric film of a capacitor, since the crystal orientation in the film gathers towards desired, the magnitude of a remanence is maximized. That is, a ferroelectric capacitor with high-reliability can be obtained.